Asynchronous Design using NULL Convention Logic

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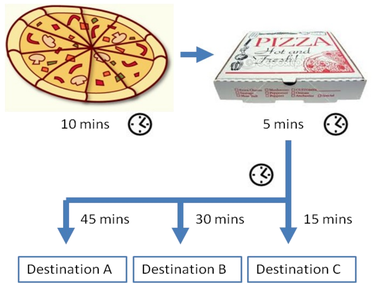
Motivation

- Digital circuits designed using asynchronous logic have advantages over clocked designs such as :
  - No clock skew
  - Lower power consumption
  - Lower noise and EMI problems
  - No global timing issues
  - Better performance in extreme temperatures
- Designing asynchronous circuits can be challenging but the advantanges cannot be ignored

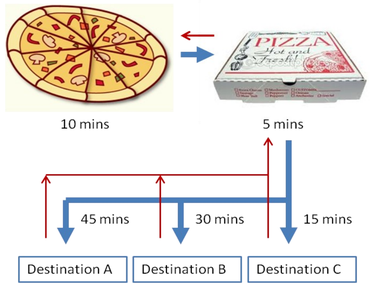
Key idea : If clock is the bottleneck then eliminate it!

Pizza store modeled like clocked digital circuits



Any new pizza can be sent for delivery only after 45 minutes

Actual model of pizza store. Asynchronous



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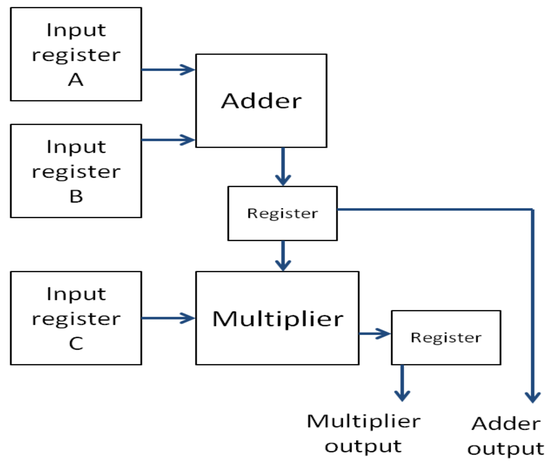
Circuit Designs

Clocked Circuit Design



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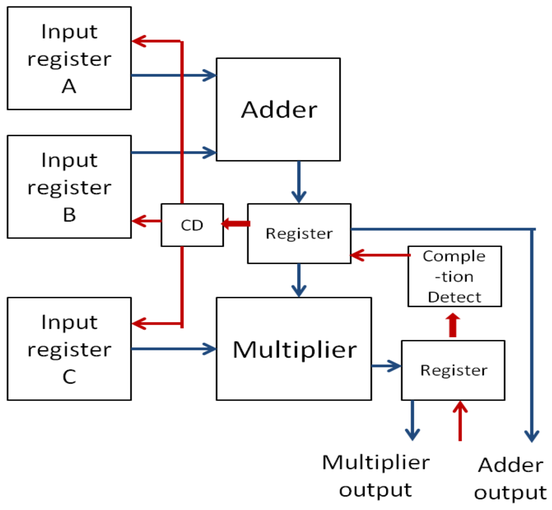
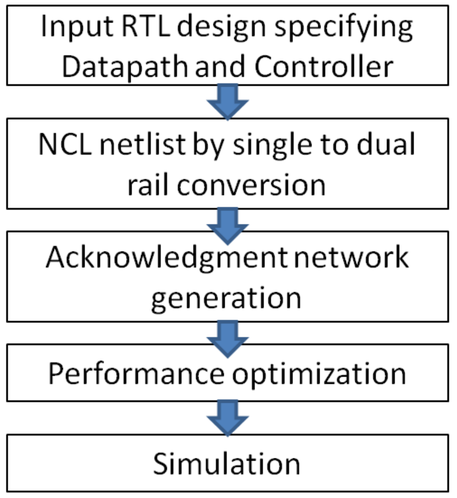


Design Steps



Work In Progress

- Toolset to generate netlist for asynchronous NCL circuit
- We now have a prototype which maps a specific format circuit data to NCL gates
- Area optimization algorithms to reduce the total number of gates needed for an NCL design are being researched.